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(54) Circuit board

(57) A fine pitch pattern multilayer printed circuit board has laminar stackable board layers providing power distribution, signal distribution and capacitive decoupling. The board layers may be fabricated by beginning with a metallic core 1, patterning the core, selectively enclosing the core in a dielectric 6, selectively depositing metal 12 to form vias 13, plugs 14 and signal lines 16, and forming dendrites 19 with joining metallurgy on the vias and plugs to provide stackable connections from above or below the plane of the board layer. In addition, a sol-gel process may be used to form a thin high dielectric constant crystalline film 27 onto a metallic sheet 26 followed with a deposition of a metallic layer 29 onto the high dielectric constant film. The film serves as the dielectric of a capacitor layer which is thereafter in succession patterned, covered by a dielectric 40, and has selectively deposited a metallic layer 42 for interconnecting the capacitor and forming vias 37, 38. The ends of the vias are thereafter subject to dendritic growth and joining metallurgy to provide stackable interconnection capability. A multilayer composite laminar stackable circuit board structure is created using, as appropriate, layers having metallic cores and layers having capacitively configured cores. The multilayer laminar stackable circuit board provides direct vertical connection between surface mounted electronic components and the power, signal and capacitive decoupling layers of the composite board through the dendrites and joining metallurgy of the via and plug formations.

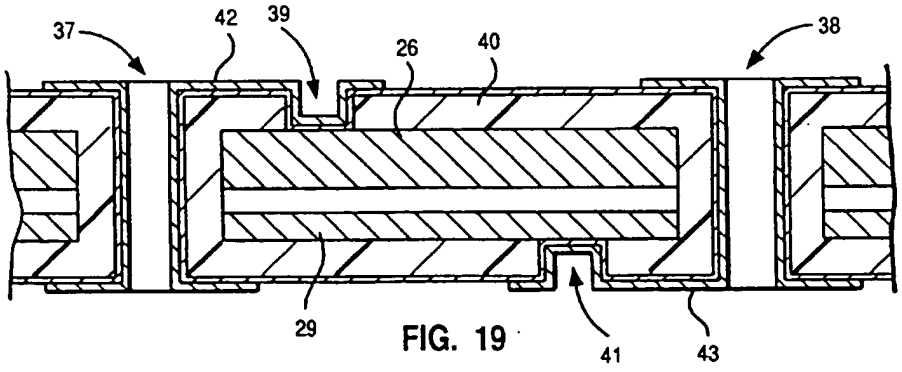

FIG. 19

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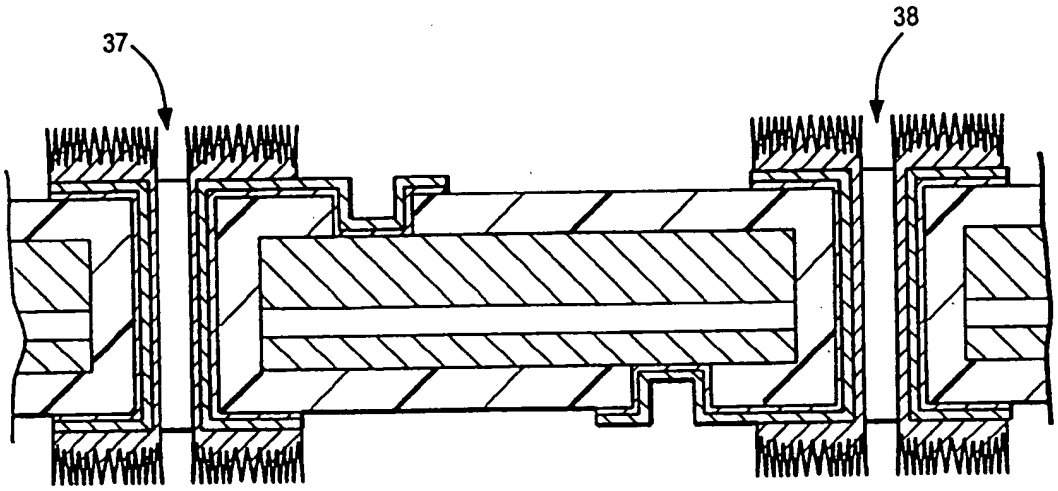

FIG. 20

Description

The present invention relates generally to electronic circuit board structures and their fabrication, and in particular to the efficient manufacture and use of circuit boards which are conveniently laminated through stacked interconnection, including circuit boards incorporating capacitive structures.

Fine pitch pattern multilayer printed circuit boards are routinely used to interconnect integrated circuit devices in complex electronic apparatus, including but not limited to computer systems. As the pitch of the conventionally used copper patterns in the various layers of the boards decreases, the layer-to-layer interconnection has proven to be more challenging when accomplished through the conventional practice of drilling and plating vias, including the use of blind vias or plugs.

In such multilayer boards, it is common to use planar sheets of copper as ground paths, as power supply paths and as shields between signal line layers. Integrated circuit packages routinely have decoupling capacitors mounted immediately adjacent their power supply leads, on the surface of the printed circuit board, to reduce noise.

The difficulty of manufacturing multilayer printed circuit boards in the fine wiring pitches needed for direct attach of integrated circuit die, such as exists with the flip-chip technology, led to the use of high density circuit boards or substrates as described in US Patent No. 5,146,674. The technology characterized by this patent involves the formation of individual layers, for a concluding multilayer board design, from electrically conductive planar sheets. Vias and plugs are formed in dielectrically insulated holes through the sheets. Signal lines are patterned in conductive layers deposited on dielectric layers formed over the metallic core sheet. Vertical interconnections are created through patterns of vias and plugs during the mating of successive layers by aligned compression.

Given that vias and plugs serve similar vertical interconnect functions, use of the term "via" hereafter is intended to encompass both forms of structures.

Reliable connection between the vias is accomplished through dendrites formed on the ends of the vias. The dendrites physically contact corresponding dendrites in other layer vias when the aligned layers are compressed. The formation and use of such dendrites is described in US Patent No. 5,137,461.

Further refinements in the use of such vertically interconnected board structures are described in US Patent No. 5,363,275, the subject matter of which is also incorporated by reference herein. This patent focuses on the selective lamination of numerous layers to both interconnect high density flip-chip devices as well as to provide the basic flexible cable resource for interconnecting groupings of such layers as may be used with a modularized component computer system.

Fabrication of the laminar stackable circuit boards which comprise the individual layers of the multilayer interconnect systems sought in the aforementioned US Patents 5,146,674 and 5,363,275 depend upon the process in 5,146,674 to create the individual layers. Though viable, the process is unfortunately complex and therefore costly. (Note that it is assumed that the reader of this application is familiar with the content of the above three US patents).

As digital system clock rates and the number integrated circuit die I/O lines increase, capacitive decoupling of the power supply at the leads of the integrated circuit die becomes more important. The prior art practice of mounting decoupling capacitors adjacent the integrated circuit packages is not desirable for a number of reasons. First, the use of such capacitors requires extra fabrication operations. In addition, the capacitors are relatively large in relation to contemporary integrated circuit devices. Lastly, since the capacitors are surface mounted devices, the ground and power supply connections must be routed to the surface at the capacitor leads, introducing resistance and inductance in the decoupling path.

Though capacitive structures may be incorporated into the integrated circuit die, the cost in silicon area and magnitude of capacitance obtainable seldom justify that approach.

Accordingly, the invention provides a circuit board capacitor, comprising:

an electrically conductive first power plane;
an electrically conductive second power plane;
a thin film first dielectric layer between the first and second power planes, forming a capacitor thereby;
a first via extending through the first power plane, the second power plane and the first dielectric layer, electrically connected to the second power plane and electrically insulated from the first power plane by a relatively thick second dielectric layer; and
a second via extending through the first power plane, the second power plane and the first dielectric layer, electrically connected to the first power plane and electrically insulated from the second power plane by the relatively thick second dielectric layer.

In a preferred embodiment, the first and second vias have dendrites at ends of the vias, the first dielectric layer is a high dielectric constant crystalline thin film, and the dendrites include a joining metallurgy. Preferably the second dielectric is a photolithographically patterned formation.

Such a circuit board capacitor may be readily extended by:

an electrically conductive third power plane;
an electrically conductive fourth power plane;
a thin film third dielectric layer between the third and fourth power planes;

a third via extending through the third power plane, the fourth power plane and the third dielectric layer, electrically connected to the fourth power plane and electrically insulated from the third power plane by a fourth dielectric layer;
a fourth via extending through the third power plane, the fourth power plane and the third dielectric layer, electrically connected to the third power plane and electrically insulated from the fourth power plane by the fourth dielectric layer; and
a direct connection between the first and third vias and between the second and fourth vias.

Thus the third and fourth power planes can be used to form a second circuit board capacitor, analogous to the first. The third and fourth vias preferably have dendrites at the ends of the vias, and the direct connection comprises physical bonding of via dendrite joining metallurgy.

Such a circuit board capacitor can also be extended by:
an electrically conductive third power plane;
a relatively thick third dielectric over the conductive third power plane;
a third via extending through the third dielectric and either side of the third power plane, electrically connected to a region of the third power plane;
a fourth via extending through the third power plane and electrically insulated from the third power plane by the relatively thick third dielectric;
a direct connection between the first and the third or fourth vias; and
a direct connection between the second and the third or fourth vias.

The invention further provides a method of making a circuit board capacitor, comprising the steps of:

forming a relatively thin film first dielectric layer on an electrically conductive first power plane;
forming an electrically conductive second power plane over the first dielectric layer;
forming a first via through the composite of the first power plane, the first dielectric layer and the second power plane, electrically connected to the second power plane and electrically insulated from the first power plane by a relatively thick second dielectric layer; and
forming a second via through the composite of the first power plane, the first dielectric layer and the second power plane, electrically connected to the first power plane and electrically insulated from the second power plane by the relatively thick second dielectric layer.

It is preferred that there are dendrites at the ends of the vias, and the step of forming a thin film first dielectric layer comprises the steps of:

depositing a sol-gel material on the first power plane; and
annealing the sol-gel material to form a high dielectric constant crystalline thin film layer.

It is further preferred that the step of forming the first and second vias comprises the steps of:

forming holes through the composite;
forming a selectively thick second dielectric layer over the first power plane, second power plane and the holes through the composite;
removing the second dielectric layer from selected areas over the first and second power planes; and
selectively forming electrically conductive vias, using the holes through the composite, onto the selected areas of the first and second power planes.

The invention further provides a method of fabricating a stackable circuit board layer, comprising the steps of:

forming holes through a metallic sheet;
forming a first dielectric layer over the metallic sheet;
forming first and second holes through the first dielectric layer at respective first and second locations;
selectively forming deposits of metal at the first and second locations, whereby the deposits of metal at the first location form a via electrically insulated from the metallic sheet by said first dielectric and the deposits of metal at the second locations form a via electrically connected to the metallic sheet; and
forming dendrites at the ends of the vias.

Preferably the method further comprises the step of forming a joining metallurgy on the dendrites, and the step of selectively forming deposits of metal comprises the steps of:

masking non-selected areas of the metallic sheet and first dielectric layer; and
plating the metal on areas not covered in the masking step.

It is further preferred that the metallic sheet comprises a copper-invar-copper composition, and the method further comprises the steps of:

forming a commoning layer before the step of plating; and
removing exposed commoning layer after the step of plating.

It is desirable that the step of selectively forming de-

posits of metal provides a formation at a third location on the first dielectric layer electrically insulated from the deposits of metal at the first and second locations.

It is also preferred that the step of forming dendrites compris s the steps of:

selectively masking areas other than the ends of the vias; and

subjecting unmasked areas to dendritic growth.

Such a process is suitable to create the individual layers of an advanced laminar stackable circuit board structure. Moreover, the capacitive structure described above can be integrated into multilayer printed circuit boards and has a fabrication process which can follow the basic tenets of the process used to create the advanced laminar stackable circuit board configurations.

The individual board layers may be stacked for electrical connection through the dendrites at the ends of the vias so that the resulting multilayer board has a laminar configuration preferably including capacitor layers, ground planes, power planes and signal lines. The vias may be fabricated in the fine pitch patterns of surface mount devices, such as ball grid array flip-chip devices.

According to one embodiment of the invention, a capacitive structure printed circuit board layer is formed, as an element of a stacked multilayer circuit board, using a thin layer of high dielectric constant sol-gel based crystalline film. Connections to the electrically conductive layers that compose the capacitor's plates are made through vias. The multiple layers of the composite board are stacked for electrical connection through the dendrites at the ends of the vias. The resulting multilayer board has a laminar configuration of capacitor layers, ground planes, power planes and signal lines. The vias are fabricated in the fine pitch patterns surface mount components, such as ball grid array flip-chip devices. The circuit board capacitors decouple the power supply at the pads of the flip-chip die, with minimum resistance and inductance in any connecting lines.

The process used to fabricate the circuit board capacitors is a refinement of the process for forming the circuit board layers which are used to provide power, ground and fine pitch signal lines in a laminar stackable circuit board format.

Preferred embodiments of the invention will now be described in detail by way of example only with reference to the following drawings:

Figs. 1-10 depict by schematic cross-section various stages during the fabrication of a circuit board layer having a power plane and signal lines.

Figs. 11 and 12 depict by schematic cross-section the preparation and laminar connection of two power plane circuit board layers.

Figs. 13-20 depict by schematic cross-section the various stages in the formation of a circuit board capacitor structure.

Fig. 21 depicts by schematic cross-section the laminar interconnection of two circuit board capacitor layers.

Fig. 22 depicts by schematic cross-section the us of a four layer laminar stackable circuit board structure to convey ground, power, and signals to a flip-chip type electronic component, the composite structure including signal layers, power supply layers, and capacitive layers, interconnected through successive via and plug structures.

Preferred embodiments of the invention will now be described, firstly with reference to the structure and fabrication of a conductive core circuit board layer, secondly with reference to the structure and efficient fabrication of capacitor core circuit board structures, and lastly with reference to a laminar stackable multilayer circuit board structure having both signal, power supply, and capacitor layers efficiently integrated into a composite which is suitable for connecting fine pitch surface mount components, such as flip-chip devices or the like.

Fabrication begins as shown in Fig. 1 with a core sheet 1 of copper-invar-copper (CIC) approximately 0.025 millimeters thick. Though less desirable, the metallic core could be composed of pure copper, chromium, invar, molybdenum, or copper-molybdenum-copper. The core is covered by a photolithographically patterned mask 2 so as to expose areas 3 to etchants such as cupric chloride and hydrochloric acid. Fig. 2 shows the CIC layer following the etch of areas 3, showing holes 4, preferably circular, extending through the sheet of CIC. The patterned sheet of CIC is then coated on both sides with a relatively thick dielectric 6 of a photoimagable polymer, such as epoxy or polyimide, as shown in Fig. 3.

Photolithographic masking and etching of dielectric 6 follows to create holes 7 as shown in Fig. 4. Standard etchants are used. Note that holes 7 are electrically insulated from CIC sheet 1 by walls of dielectric 6 while the etched openings 8 expose CIC sheet 1. An electrically conductive commoning layer 9 of copper is then conformally deposited to a nominal thickness of 0.001 to 0.0025 millimeters meters on all exposed surfaces, as shown generally in Fig. 5. Commoning layer 9 is used to facilitate plating of selected regions during a subsequent operation.

Mask 11 is then photolithographically formed over copper layer 9 to selectively expose those areas which are to be plated, as shown in Fig. 6. Following the plating and stripping of mask 11, the regions not covered by mask 11 have a nominal 0.015 to 0.05 millimeter thick layer 12 of electrically conductive copper deposited, as illustrated in Fig. 7. Note with reference to Fig. 7 that the circuit board layer at this stage in the fabrication process includes relatively thick deposits of copper on the inner walls of holes 13, on the dielectric walls and exposed areas of CIC sheet 1 at openings 14, and as selectively patterned lines on one or more surfaces of the circuit board layer, such as freestanding signal line pattern 16 or extension 17 of hole pattern 13. Such conductive re-

gions define the electrical paths within and between the layers of the laminar stackable circuit board eventually created.

Next, mask 18 is photolithographically patterned to cover all but the ends of the vias defined at 13 and the via like plug structures defined at 14. The purpose of mask 18 is to define regions for selective growth of dendrites as taught in US Patent No. 5,137,461. Fig. 9 depicts the cross-section of the board layer following the dendritic growth process, whereby dendrites 19 are formed at the opposite ends of the vias at 13 and dendrites 21 extend over both ends of the via-like plugs at 14. Note that dendrite material is also deposited along the inner passages of the vias at 13, though dendrite formation is significantly less pronounced. Plating of the dendritic regions with a joining metallurgy follows, typically using a tin/lead alloy and providing a layer nominally 0.0025 to 0.025 millimeters thick.

Fig. 10 depicts the cross-section of the layer following the stripping of mask 18 and etched removal of exposed copper commoning layer 9. Fig. 10 represents a completed layer of the stackable laminar circuit board structure. As shown in this figure, the layer includes a conductive inner core 1 suitable to supply power or ground potential through the dendritically terminated plugs at 14 from above or below the respective dendrites. Also present in the layer structure are the vias at 13, which vias likewise are available for dendritic connection from above or below the layer. Note that the vias are electrically isolated from electronically conductive core sheet 1. However, one of the vias is connected to conductor 22 on the upper surfaces of the board layer. Thereby, surface conductors such as 22, are interconnected from above or below the board layer through the dendritic termination of the vias at 13. The board layer in Fig. 10 also shows an electrically isolated conductive line 23 on the upper surface of the board. Surface conductor 23 illustrates that signal lines on the surface of the board layer can be patterned electrically distinct from the vias at 13 and plug structures at 14.

Figs. 11 and 12 depict the use of the stackable circuit board layer in Fig. 10 to create a multiple layer circuit board. In Fig. 11, the board layer is shown coated with a viscous dielectric 24. Thereafter, a second board layer, typically having a different surface conductor pattern, is aligned and mated under pressure and heat to form, as depicted in Fig. 12, a two layer stacked circuit board structure. The use of heat during the lamination step reflows the joining metallurgy on the via dendrites to form a high integrity electrical connection. The stacked structure provides a direct connection between the respective core conductors through the plug structures and direct connection of the vias and associated signal lines. The dendrites ensure reliable electrical connection while the viscous dielectric seals the boundary and binds the two stackable layers.

Considering now the formation of capacitive elements into the fundamental core structures of stackable circuit board layers, the board capacitor structures described below are particularly valuable due to (1) the exceptional size of the capacitance, attributable to the use of thin film high dielectric constant materials, (2) the optimized electrical characteristics of the connections between the capacitor structures and surface mounted electronic devices, (3) the similarity of the fabrication processes used to form capacitor structures to those processes used to fabricate other stackable board layers and (4) the ease with which multiple capacitive board layers can be connected with signal and power stackable board layers. The capacitor structure stackable board layers provide high capacitance, low resistance, low inductance structures which can be used in conjunction with the dendritically interconnected laminar stackable multilayer board described with reference to Fig. 12. The decoupling effect of the capacitive regions is particularly pronounced in that the capacitance is distributed, as defined by the array of vias, and is separated from the device leads by no more than the board layers along the via paths.

The fabrication process of the capacitor structure board layer begins as illustrated in Fig. 13 with the coating of a conductive metallic sheet 26, analogous to CIC sheet 1, with a solution-sol-gel (sol-gel) compound 27. Sheet 26 is preferably platinum plated invar, or copper-invar-copper covered by a flash coating of platinum to eliminate copper oxidation and reaction with the sol-gel compound. Sol-gel compound 27 is spin coated, sprayed, dipped or otherwise deposited onto the surface to a nominal thickness of approximately 0.001 millimeter. A variety of materials can be used for compound 27, an example being lead-lanthanum-titanate as described in IBM Research Report RC 19550 (84975) 4/25/94, entitled "Thickness Dependent Dielectric Properties of Sol-Gel Prepared Lead Lanthanum Titanate Films" by authors Beach et al, as published by the IBM Research Division, T.J. Watson Research Center. The fundamental concepts underlying the sol-gel process are described in two articles published in the technical journal Advanced Materials. The first is entitled "Advanced Dielectrics: Bulk Ceramics and Thin Films" by authors Hennings et al, as appeared in Advanced Materials 3 (1991), No. 7/8, on pages 334-340. The second article is entitled "Sol-Gel Processes" by Reuter, as appeared in Advanced Materials 3 (1991), No. 5, pages 258-259.

The next step in the sol-gel process is depicted generally in Fig. 14, comprising a high oxygen environment thermal anneal involving temperatures nominally approaching 700 degrees C. The goal is to form a thin crystalline film layer 27 on metallic sheet 26, which layer 27 is characterized by a low leakage current and an extremely high dielectric constant, typically in the range of 500. One skilled in physics will immediately appreciate a number of factors associated with dielectric layer 27. First, since the value of capacitance is inversely proportional to the thickness of the dielectric, the thin film character of dielectric layer 27 provides a structure of high

capacitance per unit area. The high capacitance also benefits from the fact that capacitance is directly proportional to the area, which now extends substantially over the full surface of the stackable circuit board layer. Lastly, since capacitance is directly proportional to the dielectric constant, the exceptionally high dielectric constant of the sol-gel formed crystalline thin film materials further accentuates the capacitance obtainable.

It should not be overlooked that the high temperatures required of the sol-gel process to form the crystalline thin films such as 27 are outside the realm of capability for convention printed circuit board compositions such as FR4. Such printed circuit board materials have a glass transition temperature in the range of 120 to 180° C. In contrast, the thermal anneal temperature of the sol-gel is suitable for metal sheet core structures such as 26, when the oxidation and reaction characteristics of the selected metal are consistent with the thermal environment.

Following the sol-gel process formation of crystalline thin film layer 27, layer 27 has deposited thereon by chemical vapor deposition, sputtering, evaporation, or plating, generally 31, a several micron thick layer of electrically conductive material 29, as schematically depicted in Fig. 15. The concluding three-layer capacitive structure in Fig. 15 then serves as the core sheet for a board layer fabrication process analogous to that described beginning with Fig. 1.

The capacitor board layer pattern formation begins with the operations which produce the cross-section depicted in Fig. 16. As shown, capacitive core sheet is selectively covered by a photolithographically processed mask 33 so as to provide openings 34 and 36. Openings 34 and 36 are preferably circular in shape. Etching of the capacitor core sheet follows, preferably employing an anisotropic etchant such as cupric chloride and hydrochloric acid. Upon the conclusion of the etch and a strip of mask 33, the core sheet appears as shown in Fig. 17 with holes at selected locations 34 and 36.

Next, a dielectric such as 6 in Fig. 3 is formed over the core sheet. A selective removal of dielectric 6 by photolithographic masking and selective etching forms a dielectrically insulated via hole at 37, a dielectrically insulated via hole at 38, an exposed contact opening at 39 to metallic layer 26 of the capacitive core, and an opening 41 through dielectric 40 to the other metallic layer 29 of the capacitive core. Processing analogous to that described with reference to Figs. 5, 6 and 7 follows, thereby producing the structure in Fig. 19. The processes include the formation of a thin copper commoning layer, the formation of a mask, and a plating to form a thick metallic layer through the vias at 37 and 38 and into the respective openings at 39 and 41, the latter formations being electrically common to effective capacitor plates 26 and 29. After the strip of the mask, the capacitor layer circuit board structure appears as shown in the cross-section of Fig. 19.

Note that plated conductive layer 42 extends through the opening at 37 to the other side of the board from a contact to conductive plate 26 of the capacitor structure at opening 39 in dielectric 40. Similarly, plated metallic layer 43 extends through the opening at 38 and is electrically connected to capacitor plate 29 through the contact opening at 41.

A photolithographic masking and dendrite formation operation, analogous to that described with reference to Figs. 8, 9 and 10, produces the capacitive circuit board layer structure depicted in Fig. 20. Note that the dendrite covered via at 37 is common to one plate of the capacitor structure while the dendrite covered via at 38 is common to the opposite plate of the capacitor structure.

A parallel connection of multiple capacitor layers produces the structure in Fig. 21. A viscous dielectric 39 is used in the manner described with reference to Fig. 12, to seal and bind the two mated circuit board layers. Again, the use of heat during the lamination step reflows the joining metallurgy on the via dendrites to form a high integrity electrical connection.

A noteworthy feature about the composite in Fig. 21 is the ease with which circuit board capacitive structures are connected in parallel, and in such form are available for further interconnection to successive signal and power distribution layers from either below or above. Note particularly that the manufacturing processes used to create the capacitive layers are similar to those practiced to create the signal and power distribution circuit board layers.

A third aspect of this approach concerns the ability to interconnect the circuit board layers which distribute the electric power and electrical signals with the layers which provide capacitive decoupling in a laminar stackable multilayer circuit board configuration. An example is shown in Fig. 22. As depicted in the figure, the composite structure has the two capacitor layers of Fig. 21 situated at the bottom of the structure in Fig. 22, and two layers of Fig. 12, which distribute the electrical signals, distribute the electrical power and provide shielding, laminated above. In the furtherance of distributing the capacitance, it likely that arrays of vias may be used to interconnect capacitive board layers without being used for further direct interconnection as component power supply and ground lines. For purposes of illustration, laminar stackable multilayer circuit board 41 is shown in anticipation of a further connection to balls 42, 43 and 44 of a ball-grid array type flip-chip electronic component 46. Note in particular that the power supply via at 47 and the ground via at 48 are situated in immediate vertical alignment with the respective balls 42 and 44. This minimizes any resistive and inductive effects which might reduce the decoupling provided by the underlying capacitive layers of the multilayer board structure. Similarly, note that electronic component ball 43 receives signals from the multilayer board connections directly below. This arrangement reduces the length of the signal path as well as any resistance or inductance in the

signal path.

Claims

1. A circuit board capacitor, comprising:

   an electrically conductive first power plane (26);
   an electrically conductive second power plane (29);
   a thin film first dielectric layer (27) between the first and second power planes, forming a capacitor thereby;
   a first via (38) extending through the first power plane, the second power plane and the first dielectric layer, electrically connected to the second power plane and electrically insulated from the first power plane by a relatively thick second dielectric layer (40); and
   a second via (37) extending through the first power plane, the second power plane and the first dielectric layer, electrically connected to the first power plane and electrically insulated from the second power plane by the relatively thick second dielectric layer.

2. The circuit board capacitor of Claim 1, wherein the first and second vias have dendrites at ends of the vias.

3. The circuit board capacitor of Claim 2, wherein the first dielectric layer is a high dielectric constant crystalline thin film and the dendrites include a joining metallurgy.

4. The circuit board capacitor of any preceding Claim, wherein the second dielectric is a photolithographically patterned formation.

5. The circuit board capacitor of any preceding Claim, further comprising:

   an electrically conductive third power plane;
   an electrically conductive fourth power plane;
   a thin film third dielectric layer between the third and fourth power planes;
   a third via extending through the third power plane, the fourth power plane and the third dielectric layer, electrically connected to the fourth power plane and electrically insulated from the third power plane by a fourth dielectric layer;
   a fourth via extending through the third power plane, the fourth power plane and the third dielectric layer, electrically connected to the third power plane and electrically insulated from the fourth power plane by the fourth dielectric layer; and
   a direct connection between the first and third vias and between the second and fourth vias.

6. The circuit board capacitor of Claim 5, wherein the third and fourth vias have dendrites at the ends of the vias, and wherein the direct connection comprises physical bonding of via dendrite joining metallurgy.

7. A circuit board capacitor element, comprising:

   a circuit board capacitor as claimed in any preceding claim;
   an electrically conductive third power plane;
   a relatively thick third dielectric over the conductive third power plane;
   a third via extending through the third dielectric and either side of the third power plane, electrically connected to a region of the third power plane;
   a fourth via extending through the third power plane and electrically insulated from the third power plane by the relatively thick third dielectric;
   a direct connection between the first and the third or fourth vias; and
   a direct connection between the second and the third or fourth vias.

8. A method of making a circuit board capacitor, comprising the steps of:

   forming a relatively thin film first dielectric layer (27) on an electrically conductive first power plane (26);
   forming an electrically conductive second power plane (29) over the first dielectric layer;
   forming a first via (38) through the composite of the first power plane, the first dielectric layer and the second power plane, electrically connected to the second power plane and electrically insulated from the first power plane by a relatively thick second dielectric layer; and
   forming a second via (37) through the composite of the first power plane, the first dielectric layer and the second power plane, electrically connected to the first power plane and electrically insulated from the second power plane by the relatively thick second dielectric layer.

9. The method of Claim 8, comprising the further step of forming dendrites at the ends of the vias.

10. The method of Claim 8 or 9, wherein the step of forming a thin film first dielectric layer comprises the steps of:

    depositing a sol-gel material on the first power

plane; and
annealing the sol-gel material to form a high dielectric constant crystalline thin film layer.

11. The method of any of Claims 8 to 10, wherein the forming of the first and second vias, comprises the steps of:

forming holes through the composite;
forming a selectively thick second dielectric layer (40) over the first power plane, second power plane and the holes through the composite;
removing the second dielectric layer from selected areas over the first and second power planes; and
selectively forming electrically conductive vias, using the holes through the composite, onto the selected areas of the first and second power planes.

12. A method of fabricating a stackable circuit board layer, comprising the steps of:

forming holes through a metallic sheet (1);
forming a first dielectric layer over the metallic sheet (6);
forming first and second holes (7, 8) through the first dielectric layer at respective first and second locations;
selectively forming deposits of metal (12) at the first and second locations, whereby the deposits of metal at the first location form a via (13) electrically insulated from the metallic sheet by said first dielectric and the deposits of metal at the second locations form a via (14) electrically connected to the metallic sheet; and
forming dendrites at the ends of the vias (19, 21).

13. The method of Claim 12, comprising the further step of forming a joining metallurgy on the dendrites.

14. The method of Claim 12 or 13, wherein the step of selectively forming deposits of metal comprises the steps of:

masking non-selected areas of the metallic sheet and first dielectric layer; and
plating the metal on areas not covered in the masking step.

15. The method of Claim 14, comprising the further steps of: forming a commoning layer (9) before the step of plating; and removing exposed commoning layer after the step of plating.

16. The method of any of Claims 12 to 15, wherein the metallic sheet comprises a copper-invar-copper composition.

17. The method of any of Claims 12 to 16, wherein the step of selectively forming deposits of metal provides a formation at a third location on the first dielectric layer electrically insulated from the deposits of metal at the first and second locations.

18. The method of any of Claims 12 to 17, wherein the step of forming dendrites comprises the steps of:

selectively masking areas other than the ends of the vias; and
subjecting unmasked areas to dendritic growth.

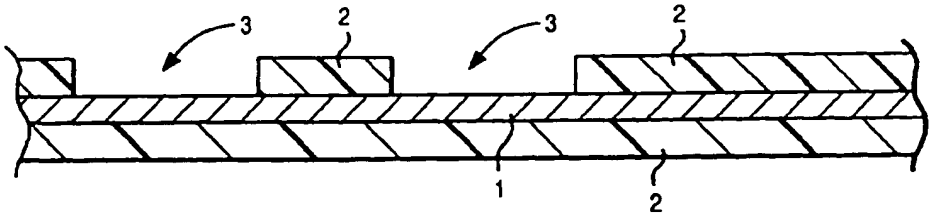

FIG. 1

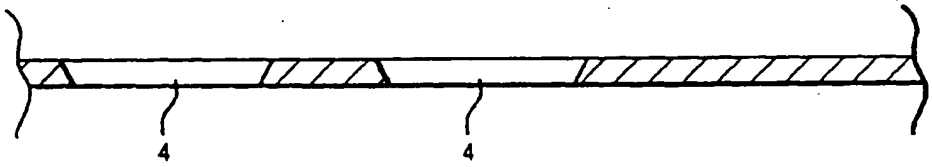

FIG. 2

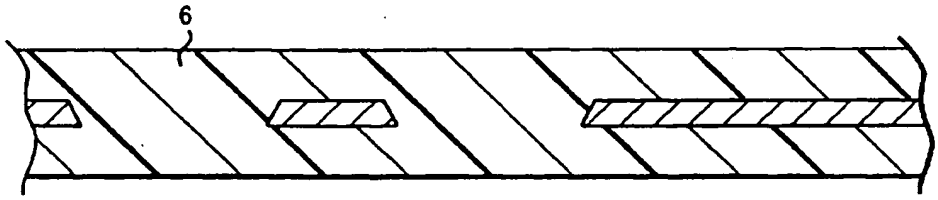

FIG. 3

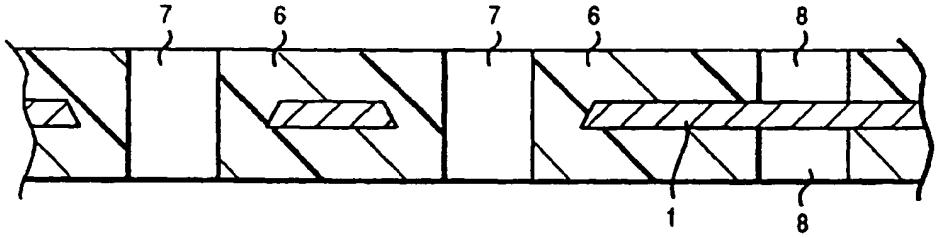

FIG. 4

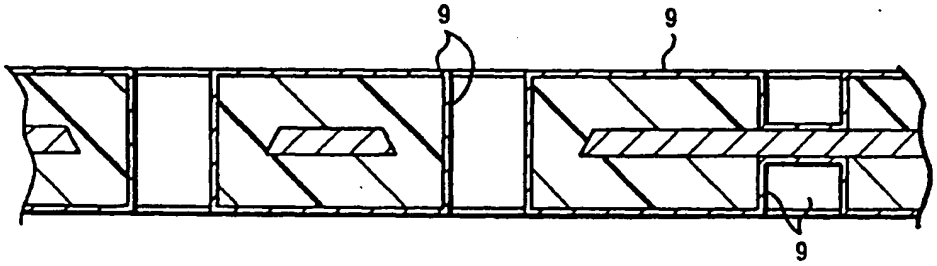

FIG. 5

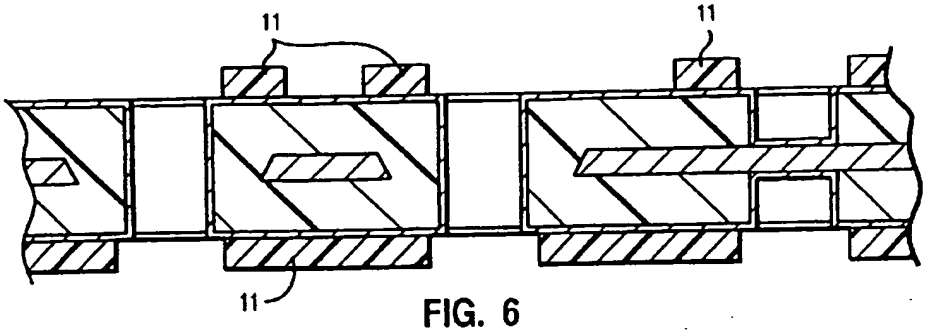

FIG. 6

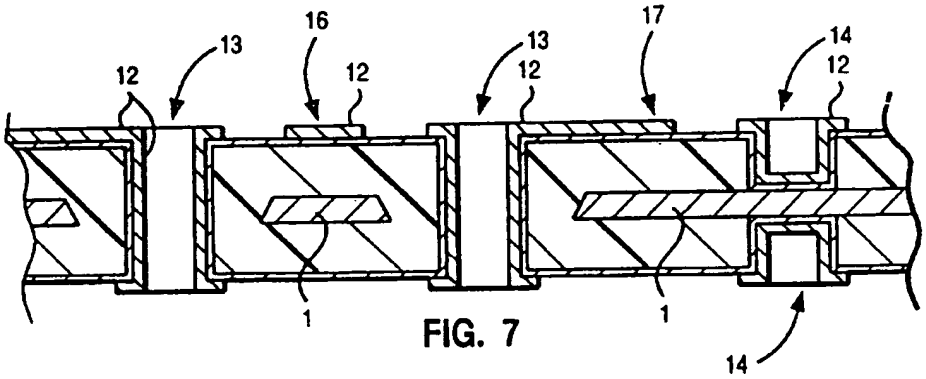

FIG. 7

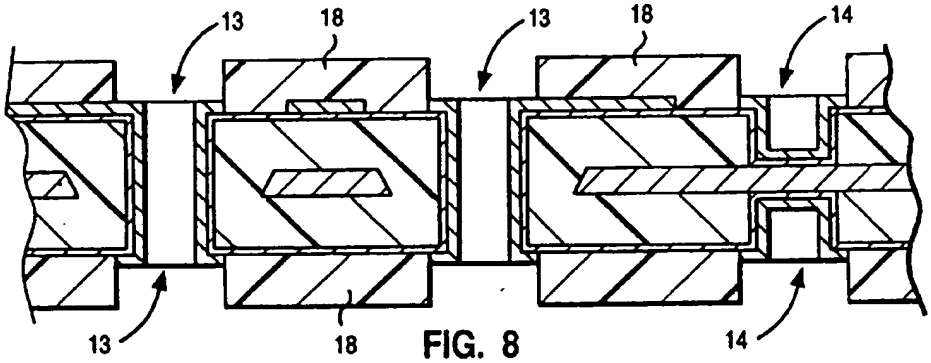

FIG. 8

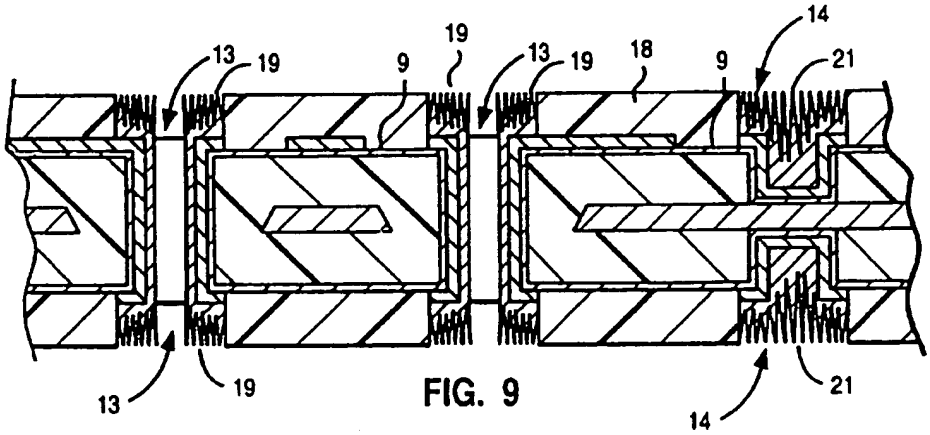

FIG. 9

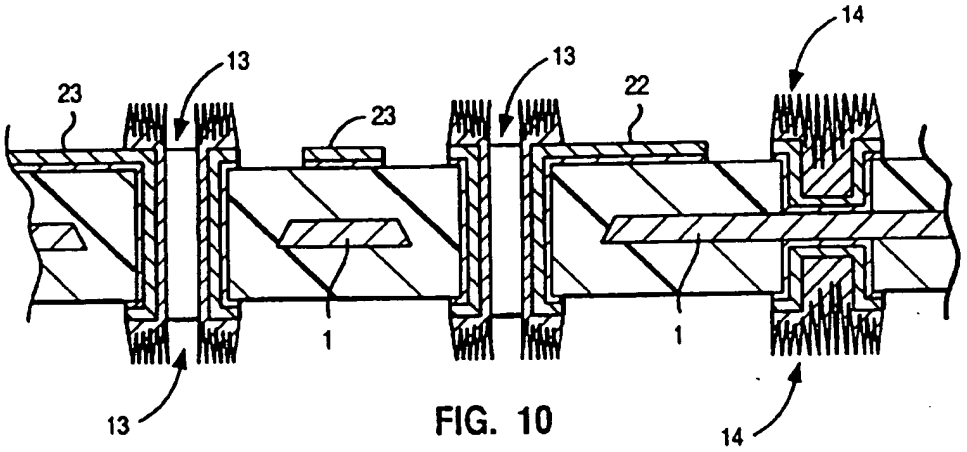

FIG. 10

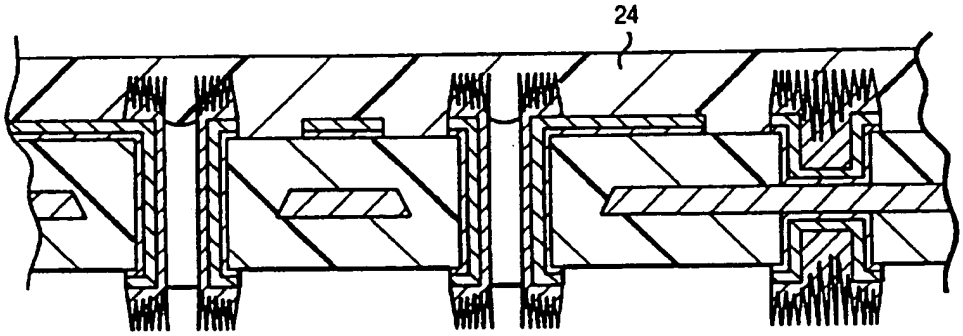

FIG. 11

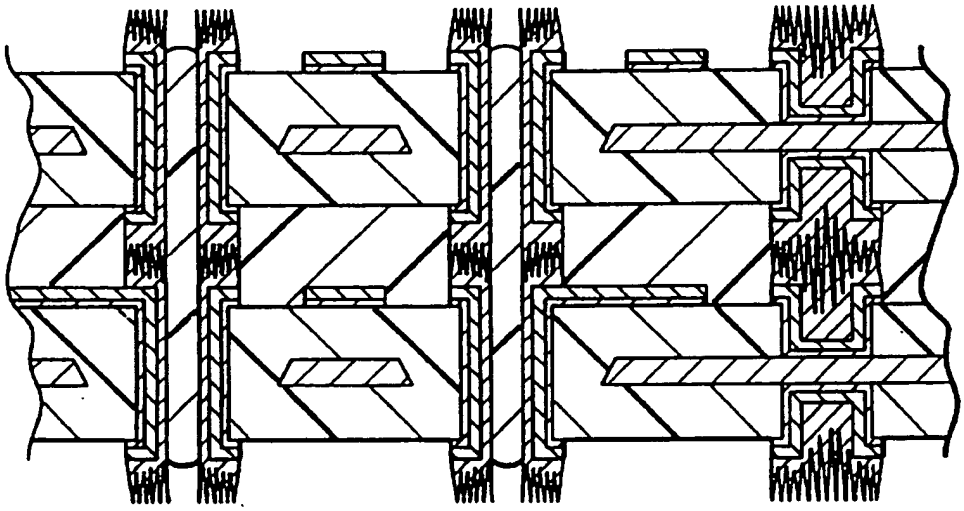

FIG. 12

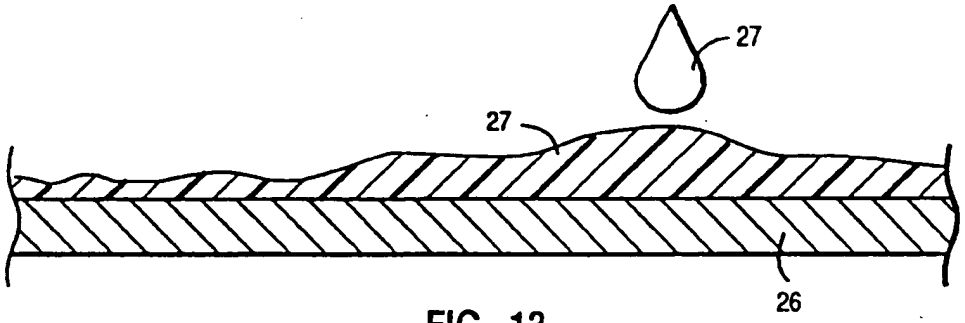

FIG. 13

(ANNEAL IN O_2)

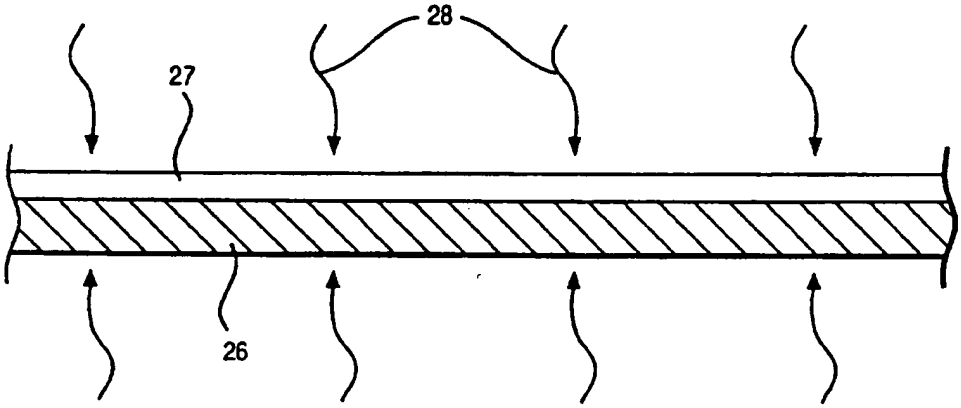

FIG. 14

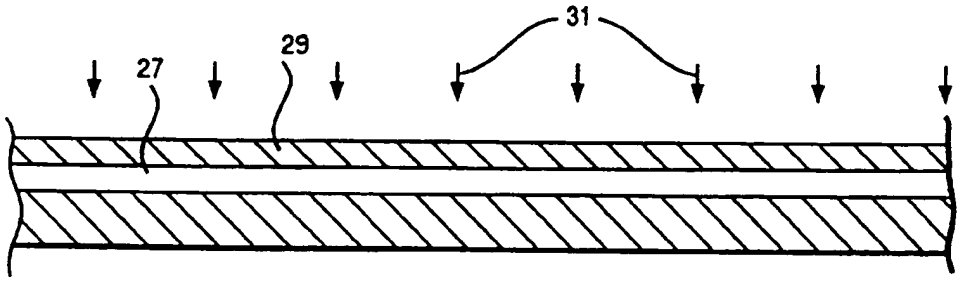

FIG. 15

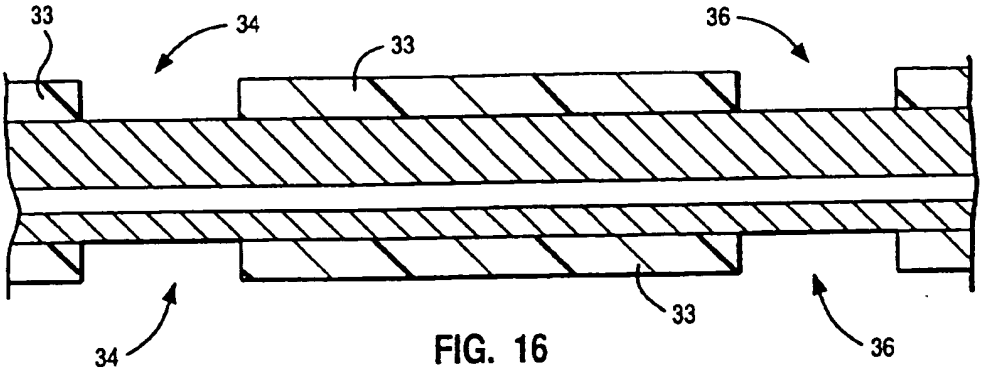

FIG. 16

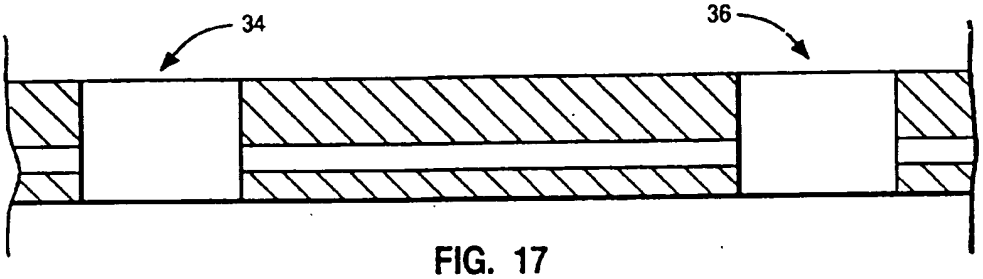

FIG. 17

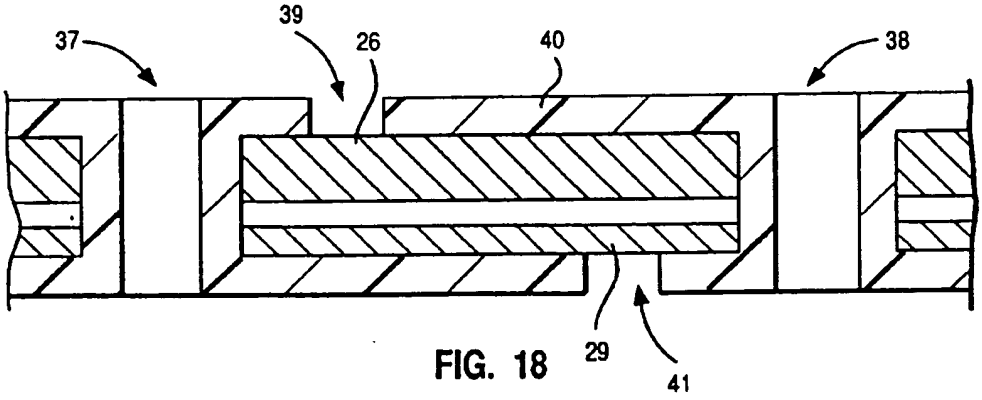

FIG. 18

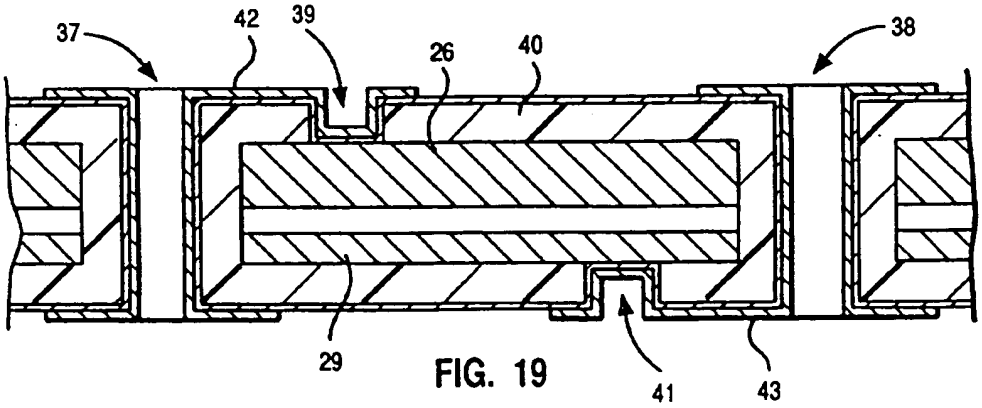

FIG. 19

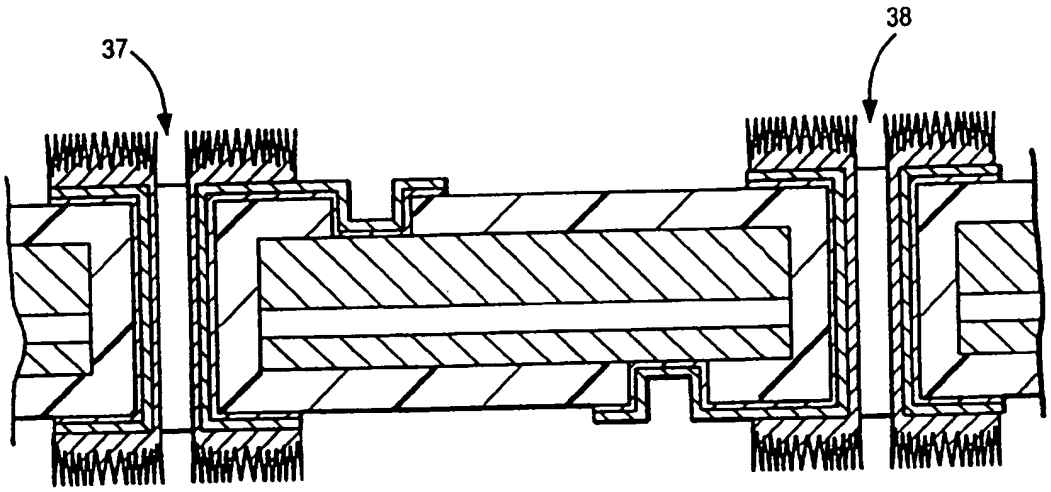

FIG. 20

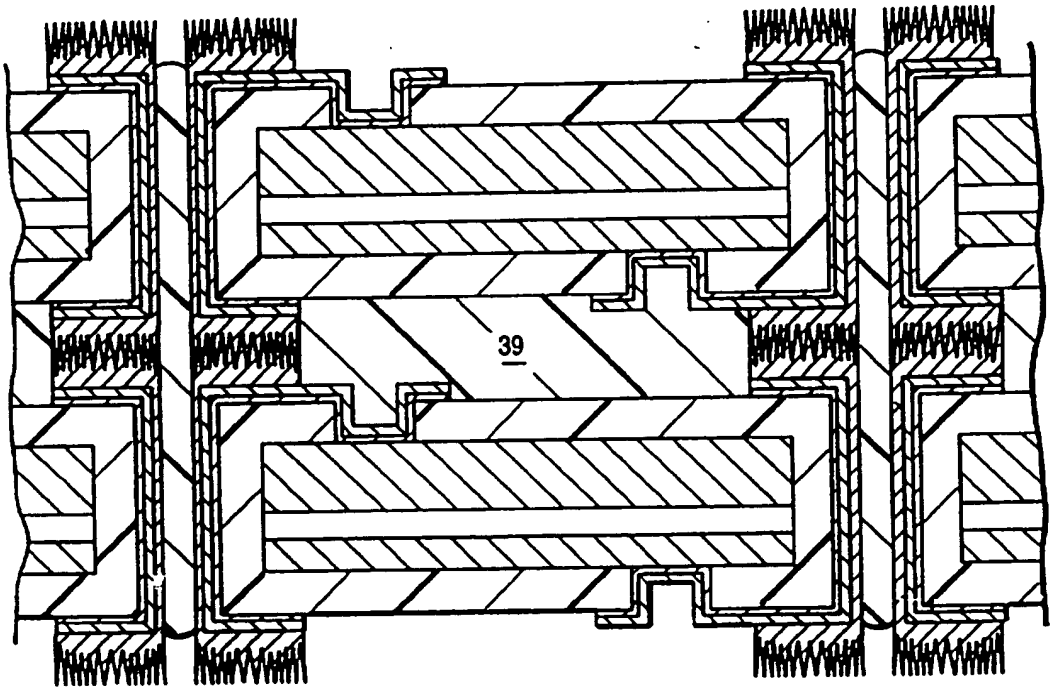

FIG. 21

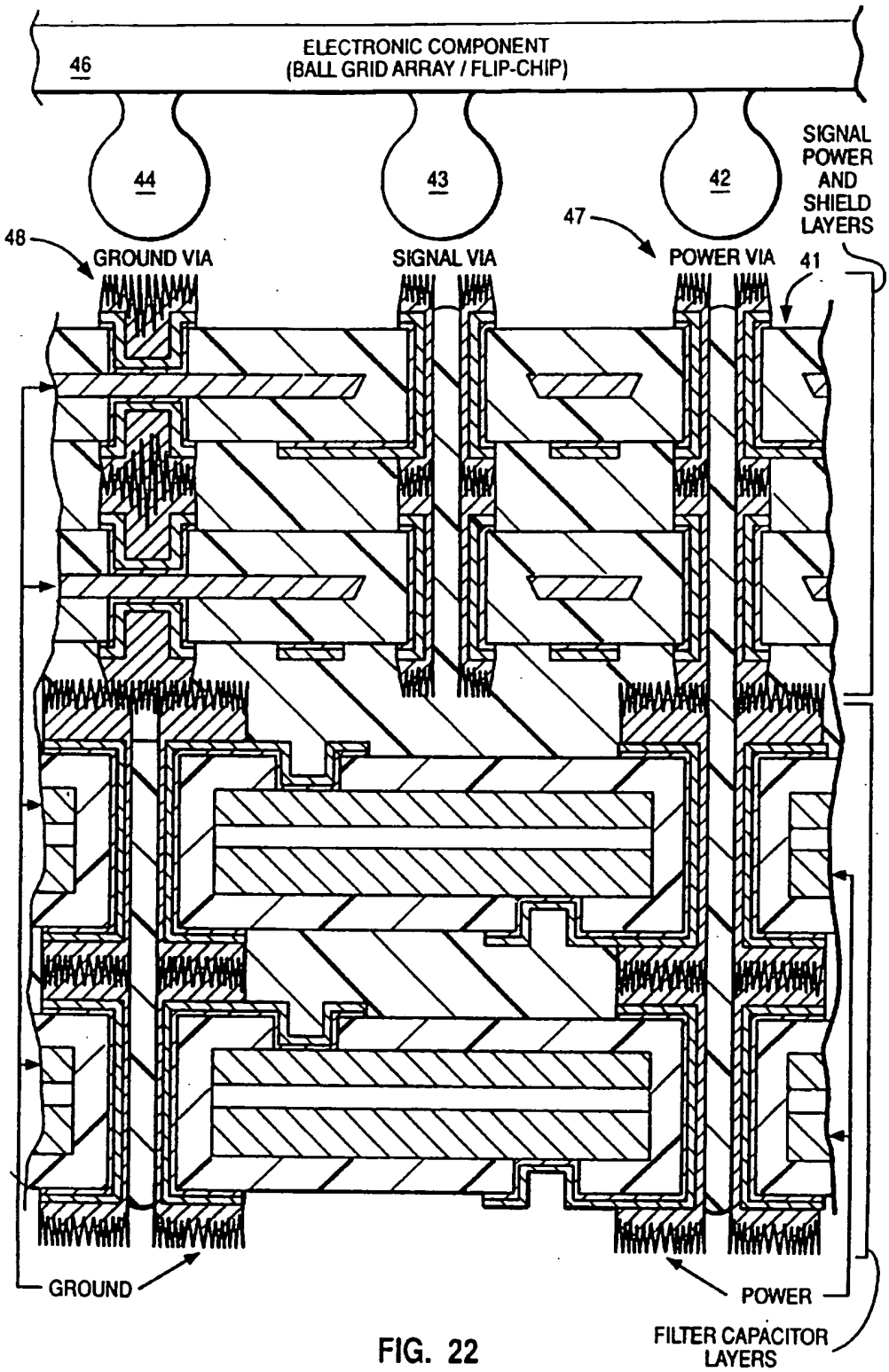
ELECTRONIC COMPONENT
(BALL GRID ARRAY / FLIP-CHIP)
46
44
43
42
SIGNAL
POWER
AND
SHIELD
LAYERS
41
48
GROUND VIA
SIGNAL VIA
47
POWER VIA
GROUND
POWER
FILTER CAPACITOR
LAYERS

FIG. 22